UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,060	08/19/2004	Rick West		9454

35619 7590 10/19/2006

DISTRIBUTED POWER
3547-C SOUTH SOUTH HIGUERA ST.
SAN LUIS OBISPO, CA 93401

EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,060	WEST, RICK	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:
Applicant evidently has executed the Declaration electronically. In accordance with 37 CFR § 1.4(d)(2), an S-signature must be inserted between forward slash marks. However, the Applicant has failed to do this by typing only "rw" in the Signature box of the submitted Declaration. The recommended correction is to provide the following formatted signature in the Signature box of the new Declaration: /Rick West/. Please see 37 CFR § 1.4(d)(2) which clearly sets forth all details regarding S-signatures.

Claim Objections

2. Claims 1 and 4 are objected to because of the following informalities:

As to Claim 1, line 14: "the said" is redundant. The word "the" should be deleted.

As to Claim 1, after the final word "mechanism" insert a period --.--.

As to Claim 4, line 2: "caries" should be changed to --carries--.

Claims 2, 3 and 5-11 depend from Claim 1 and therefore inherit the defects of the claim.

Appropriate correction is required.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The Abstract should be in narrative form and generally limited to a single paragraph on a separate sheet **within the range of 50 to 150 words**. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The Abstract of the disclosure is objected to because it is in excess of 150 words.

Correction is required. See MPEP § 608.01(b).

Drawings

5. The drawings filed on August 19, 2004 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Allowable Subject Matter

6. Claims 1-11 would be allowable if rewritten or amended to overcome the objections set forth in this Office action.

7. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 1-11, patentability resides in the limitations wherein *the bus bar major dimension runs perpendicular to the electrical current flow in the semiconductor power devices, or, where any other bus bar geometry is used that substantially serves to minimize the inductance between the semiconductor power devices on the IMS PCB and the capacitors on the filter PCB*, in combination with the other limitations of base Claim 1.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure and Examiner's reasons for indicating allowable subject matter.

a) Tamba et al. (US 6,661,659 B2) discloses a power circuit assembly comprising: (i) a modular PCB assembly 510 (i.e., a substrate with printed circuits and IGBTs mounted thereon: Fig. 6: col.6: 9-11 and 22-25) and a plurality of semiconductor power devices (IGBTs) mounted to the module substrate (col.6: 22-25); (ii) a second PCB assembly, designated filter PCB 60 (Fig. 6; col.6: 9-15), further comprising: one or more electrically conductive layers and one or more capacitors 513, 525 (col.6: 9-15); (iii) a heat removal surface (i.e., the surface of aluminum housing 61; col.6: 9-10 and col.6: 61-col.7: 3); (iv) a clamping mechanism (bolts 54, 55, 56, 57; col.6: 15-16, 29 and 35-38). Tamba et al. further teaches a bus bar geometry that minimizes mutual inductance between bus bars 517 and 518 (col.6: 29-32 and col.9: 28-30) and thereby

minimizes that part of the bus bar mutual inductance contributing to the inductance between the semiconductor (IGBT) power devices 510 and the filter capacitor 520--IGBT devices 510 **and** filter capacitor 520 being directly mounted to--and electrically connected through--bus bars 517 and 518, the connections of filter capacitors 520 and IGBTs 510 to bus bars 517, 518 effected by clamp bolts 55 and 56, respectively (Figs. 6 and 21; col.9: 37-47). **Filter capacitors 520 are not mounted to the filter PCB 60** (Fig. 6) and **not mounted** to filter PCB 58 in the other embodiments (see Figs. 5 and 7-14). Tamba et al. does not appear to teach or fairly suggest that the disclosed bus bar geometry of bus bars 517 and 518 serves to minimize an inductance effect between semiconductor (IGBT) power devices 510 and the filter capacitors 513 **on the filter PCB 60** (Fig. 6; col.6: 9-14) and does not teach or fairly suggest that any such inductance effect between semiconductor power devices 510 (IGBTs mounted on a module substrate) and capacitors 513 mounted on filter PCB 60 exists as a problem to be solved by the disclosed structural arrangement and geometry of bus bars 517 and 518.

b) Reichard (US 6,459,605 B1) discloses a power circuit assembly 23 comprising: first and second power buses 28, 32, components inclusive of power semiconductors, not shown, on first circuit board 42, and bus sheet 60 (Fig. 5) or sheets 60 and 66 on second circuit board 56 (Figs. 7 and 8). The bus sheet 60 or sheets 60, 66 on second circuit board 56, in conjunction with buses 28, 32 on first circuit board 42 form distributed bus structures that minimize overall inductance in the power circuit assembly 23. Reichard does not teach that the major dimension of the bus bars 28, 32

runs perpendicular to the current flow in the semiconductor power components on first board 42.

c) Rinehart et al. (US 6,359,331 B1) discloses stray bus inductance within a power circuit assembly (col.3: 6-14) that is minimized by placing a decoupling capacitor C_d directly across selected leads of the power semiconductors (col.3: 55-col.4: 5). Rinehart et al. additionally teaches that the power circuit assembly disclosed facilitates various types of power circuits, e.g., half bridge, full bridge, three-phase bridge, etc. (col.4: 59-65). Rinehart et al. does not teach a geometry of the buses that serves to minimize an inductance effect between the power semiconductors and the capacitor C_d and does not teach that any such inductance effect between capacitor C_d and the power semiconductors exists as a problem to be solved by a particular geometry of the buses.

d) Ahmed et al. (US 6,845,017 B2) discloses a power circuit assembly, clamped to a heat removal surface (col.5: 23-30) and including switching circuitry in half-bridge configuration (col.6: 21-22), and comprising a DC bus 31 consisting of a positive plate 57 and negative plate 59 in parallel, the positive and negative plates 57 and 59 carrying current in opposite directions and forming a capacitance therebetween, thereby canceling bus inductance and dampening voltage overshoots due to the switching occurring in the power semiconductor devices (Figs. 3 and 6; col.5: 31-36 and 45-62; col.6: 40-56). Ahmed et al. does not teach a first power semiconductor PCB and a second filter PCB with capacitors, and a bus geometry involving bus plates 57 and 59 that would minimize inductance between the power semiconductor devices on the power PCB and the capacitors on the filter PCB.

e) Hosen (US 5,497,291) discloses a power circuit assembly comprising an insulating metal substrate (IMS) 1, power semiconductors 2 (col.3: 1-5) and a conductive pattern of copper foil for mounting the power semiconductor chips 2 thereon (col.4: Claim 2). Hosen further teaches terminal plates 7 that function as bus bars through which large currents flow, wherein the geometry of terminal plates 7 is chosen in accordance with the power semiconductor chips 2 in order to enable power semiconductor chips 2 having a large capacitance to be arranged on an IMS PCB 1 having a small area (col.3: 17-20; col.3: 56-col.4: 2). Hosen does not teach the terminal plates 7 run perpendicular to the electrical current flow in power semiconductor chips 2 and does not teach filter capacitors on substrate 8 and power circuit inductance problems such that the terminal plates 7 serve to minimize any inductance effects between the power semiconductor chips 2 and any capacitors on substrate 8.

f) Nakamura et al. (US 6,784,538 B2) discloses a lead frame 1006 on a glass substrate 1007 and power semiconductors (IGBTs 1003a) mounted on the lead frame leads 1006a via solder 1020a (Figs. 1 and 7).

g) Rodriguez et al. (US 7,046,535 B2) discloses a power circuit assembly comprising a circuit board 68, for use with the half-bridge inverter module 50, with circuit wiring formed thereon using copper or aluminum foil, the advantage of using foil being that the circuit layers 72, 74 of the board 68, laminated on insulating layer 70, may be thin and thereby significantly reduce material costs and parasitic inductances (col.6: 60-67).

9. This application is in condition for allowance except for the following formal matters:

(i) Declaration defective due to incorrect S-signature format (see section 1, above).

(ii) Minor grammatical and typographical errors in the claims (see section 2, above).

(iii) Abstract in excess of 150 words (see sections 3 and 4, above).

(iv) Informalities in the Drawings determined by the Draftsperson and indicated in the attached Form PTO-948 (see section 5, above).

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on 571-272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
October 17, 2006